a channel forming region overlapped with a gate electrode; and

a fourth impurity region having the n-type conductivity and a first impurity region having the n-type conductivity which forms a source region or a drain region, wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode.

REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application.

The Examiner's Final Office Action dated April 1, 2002 has been received and its contents reviewed. Claims 1-44 and 81-85 were pending in the present application. By this amendment, claim 2 has been canceled, and claims 1, 9, 18 and 27 have been amended. Accordingly, claims 1, 3-44 and 81-85 remain pending, of which claims 1, 9, 18, 27, and 36 are independent.

Turning now to the detailed Office Action, claims 1-44 and 81-85 are rejected under 35 U.SC. §112, second paragraph, as failing to set forth the subject matter which Applicants regard as the invention. More specifically, in section 2, page 2 of the Office Action, the Examiner contends that the statement at page 8 of paper No. 13 filed 1/14/02 indicates that the invention is different from what is defined in the claims because Applicants' invention defined in the claims does not include the "5 types of transistors".

In response, Applicants respectfully submit that the statement made explained that the essence of the present invention is to optimize the structure of TFTs that constitutes each circuit in response to the respective specifications of the pixel portion and the driver portion by providing the LDD region so as to be overlapped, partially overlapped or non-overlapped with the gate electrode. In order to systematically identify various types of transistors that are used in combination with each other in an optimal way in the claimed semiconductor device, Applicants decided to use the nomenclature "first transistor", "second transistor", "third transistor", "fourth transistor" and "fifth transistor". However, Applicants never disclosed or implied that the essence of the invention requires 5 transistors. In other words, Applicants never explained that

the use of the 5 types of transistors is the essential feature of the present invention, and that the claimed semiconductor device should, could, or would concurrently have all 5 types of transistors in combination. Therefore, claims 1-8, for example, recite a "first", "fourth" and "fifth" transistor but are silent about a "second" and "third" transistor, as the Examiner has noticed. Similarly, claims 9-17, as another example, does not recite a "third" transistor, as noted by the Examiner. Furthermore, as written, the pending claims cannot be interpreted as being of the essence of having five transistors as the Examiner has incorrectly construed.

Moreover, with respect to section 3, page 3 of the Office Action, Applicants have amended claim 39, as shown above, to delete the recitation of "fourth transistor". Therefore, Applicants respectfully request reconsideration and withdrawal of the §112, second paragraph, rejection of claims 1-44 and 81-85.

Claims 1, 9, 18, 27, 36 and 81-85 are rejected under U.S.C. §103(a) as being unpatentable over applicant's admitted prior art (AAPA) in view of Hatano et al. (IEEE article - hereafter Hatano). Further, claims 2, 10-11, 19-20, 28-29, and 37-38 are rejected under U.S.C. §103(a) as being unpatentable over AAPA in view of Hatano as applied to claims 1, 9, 18, 27, and 36 above, and further in view of Mimura et al. (U.S. Patent No. 6,127,210 - hereafter Mimura). These rejections are respectfully traversed at least for the reasons provided below.

With respect to the rejection of claims 9, 27 and 36, as amended, claim 9 and 27 recite, among other things, a second thin film transistor comprising a channel forming region and a third impurity region wherein the channel forming region and the third impurity region are overlapped with a gate electrode, and a second impurity region and a first impurity region which forms a source region or a drain region wherein the first impurity region and the second impurity region are not overlapped with the gate electrode. Applicants respectfully assert that even if AAPA and Hatano et al. were combined, their combination would still be deficient in a thin film transistor comprising both an impurity region formed on the inside of a gate electrode and an impurity region formed on the outside of the gate electrode as disclosed in the amended claims.

Claim 36 recite a second thin film transistor comprising a second lightly doped drain (LDD) region formed in a second semiconductor layer so as to be partially overlapped with a

second gate electrode. Applicants respectfully submit that even if AAPA and Hatano et al. were combined, the combination would still be deficient in the LDD partially overlapped with the gate electrode as recited in claim 36.

With respect to claim 1 and 18, as amended, Applicants have added the features claim 2 to claim 1, and Applicants have added to claim 18 a feature in which the gate electrode has a first layer comprising TaN and a second layer comprising Ti on the first layer. Support for the amendment of claim 18 can be found in at least, e.g., Embodiment 1 in the present specification.

Although the dependent claim 2 was rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Hatano and further in view of Mimura in the previous Office Action, Applicants respectfully assert that Mimura does not disclose or suggest that a concentration of an impurity element included in an impurity region in a thin film transistor of a driver circuit is less than that of the impurity element included in the impurity region in the thin film transistor of a pixel section as recited in amended claim 1. Further, AAPA and Hatano et al. do not disclose the feature that the gate electrode has the first layer comprising TaN and the second layer comprising Ti as recited in amended claim 18. Therefore, amended claims 1 and 18 distinguish over AAPA and Hatano.

The requirements for establish a *prima facie* case of obviousness, as detailed in MPEP § 2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the reference themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference (or references when combined) must teach or suggest all of the claim limitations. As the AAPA and Hatano, applied separately or combined, are deficient as set forth above, the §103(a) rejections are improper.

In view of the foregoing amendments and arguments, Applicants respectfully request reconsideration and withdrawal of the §103(a) rejections.

Conclusion

Having responded to all rejections set forth in the outstanding Final Office Action, it is submitted that the claims 1, 3-44, and 81-85 are now in condition for allowance. An early and favorable Notice of Allowance is respectfully solicited. In the event that the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, the Examiner is courteously requested to contact Applicants' undersigned representative.

Respectfully submitted,

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MARKED-UP VERSION OF THE AMENDED CLAIMS

1. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit includes:

a first thin film transistor comprising:

a channel forming region and a third impurity region having n-type conductivity, [formed on the inside of] wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region is not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region[,] and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region [formed on the inside of] overlapped with a gate electrode; and a fourth impurity region having the n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode[.],

wherein an impurity element having the n-type conductivity is included in the third impurity region and in the fourth impurity region and a concentration of the impurity element included in said fourth impurity region is less than a concentration of the impurity element included in said third impurity region.

9. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having n-type conductivity, [formed on the inside of] wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region is not overlapped with the gate electrode;

a second thin film transistor comprising:

a channel forming region and a third impurity region having the n-type conductivity, [formed on the inside of] wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a second impurity region having the n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the second impurity region are not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region[,] and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

a fourth thin film transistor having:

a channel forming region [formed on the inside of] overlapped with a gate electrode; and

a fourth impurity region having the n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode.

18. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a third thin film transistor comprising:

a channel forming region [formed on the inside of] overlapped with a gate electrode; and

a second impurity region having n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the second impurity region are not overlapped with the gate electrode; and

a fifth thin film transistor comprising:

a channel forming region[,] and a fifth impurity region having p-type conductivity which forms a source region or a drain region; and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region [formed on the inside of] overlapped with a gate electrode; and

a fourth impurity region having the n-type conductivity[,] and a first impurity region the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode[.].

wherein the gate electrode has a first layer comprising TaN and a second layer comprising Ti on the first layer.

27. (Twice Amended) A semiconductor device comprising a driver circuit and a pixel section over a substrate, wherein:

a) said driver circuit comprises:

a first thin film transistor comprising:

a channel forming region and a third impurity region having n-type conductivity, [formed on the inside of] wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a first impurity region having the n-type conductivity which forms a source region or a drain region[, formed on the outside of] wherein the first impurity region is not overlapped with the gate electrode;

wherein said first thin film transistor constitutes a shift register circuit, and

a second thin film transistor comprising:

a channel forming region and the third impurity region having the n-type conductivity, [formed on the inside of] wherein the channel forming region and the third impurity region are overlapped with a gate electrode; and

a second impurity region having the n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the second impurity region are not overlapped with the gate electrode;

wherein said second thin film transistor constitutes a sampling circuit, and

b) said pixel section comprises:

a fourth thin film transistor comprising:

a channel forming region [formed on the inside of] overlapped with a gate electrode; and

a fourth impurity region having the n-type conductivity[,] and a first impurity region having the n-type conductivity which forms a source region or a drain region, [formed on the outside of] wherein the first impurity region and the fourth impurity region are not overlapped with the gate electrode.